

HIGH PERMITTIVITY SILICATE GATE DIELECTRIC

RELATED PATENT APPLICATIONS

This application claims priority from the following U.S.
5 provisional applications: No. 60/053,661, filed 7/24/97; No.
60/053,616, filed 07/24/97; and No. 60/053,617 filed, 07/24/97.

Sub 81 *09/115,855* *09/115,856*
This invention is related to concurrently filed
applications Serial No. ~~TBD (TI-25859)~~ and Serial No. ~~TBD (TI-~~
26146), which are incorporated herein by reference.

FIELD OF THE INVENTION

This invention relates generally to semiconductor device
structures and methods for forming such, and more specifically
to such structures and methods related to gate dielectrics for
15 field effect devices formed on integrated circuits.

BACKGROUND OF THE INVENTION

Semiconductor devices such as field effect transistors are
common in the electronics industry. Such devices may be formed
20 with extremely small dimensions, such that thousands or even
millions of these devices may be formed on a single-crystal
silicon substrate or "chip" and interconnected to perform useful
functions in an integrated circuit such as a microprocessor.

Although transistor design and fabrication is a highly
25 complex undertaking, the general structure and operation of a

transistor are fairly simple. With reference to Fig. 1, a simplified field effect transistor is shown in cross-section. In a field effect transistor a portion of the substrate **100** near the surface is designated as the channel **120** during processing.

5 Channel **120** is electrically connected to source **140** and drain **160**, such that when a voltage difference exists between source **140** and drain **160**, current will tend to flow through channel **120**. The semiconducting characteristics of channel **120** are altered such that its resistivity may be controlled by the
10 voltage applied to gate **190**, a conductive layer overlying channel **120**. Thus by changing the voltage on gate **190**, more or less current can be made to flow through channel **120**. Gate **190** and channel **120** are separated by gate dielectric **180**; the gate dielectric is insulating, such that between gate **190** and channel
15 **120** little or no current flows during operation (although "tunneling" current is observed with thin dielectrics). However, the gate dielectric allows the gate voltage to induce an electric field in channel **120**, giving rise to the name "field effect transistor."

20 Generally, integrated circuit performance and density may be enhanced by "scaling", that is by decreasing the size of the individual semiconductor devices on a chip. Unfortunately, field effect semiconductor devices produce an output signal that is proportional to the width of the channel, such that scaling

reduces their output. This effect has generally been compensated for by decreasing the thickness of gate dielectric 180, thus bringing the gate in closer proximity to the channel and enhancing the field effect.

5 As devices have scaled to smaller and smaller dimensions, the gate dielectric thickness has continued to shrink. Although further scaling of devices is still possible, scaling of the gate dielectric thickness has almost reached its practical limit with the conventional gate dielectric material, silicon dioxide.

10 Further scaling of silicon dioxide gate dielectric thickness will involve a host of problems: extremely thin layers allow for large leakage currents due to direct tunneling through the oxide; because such layers are formed literally from a few layers of atoms, exacting process control is required to
15 repeatably produce such layers; uniformity of coverage is also critical because device parameters may change dramatically based on the presence or absence of even a single monolayer of dielectric material; and finally, such thin layers form poor diffusion barriers to impurities.

20 Realizing the limitations of silicon dioxide, researchers have searched for alternative dielectric materials which can be formed in a thicker layer than silicon dioxide and yet still produce the same field effect performance. This performance is often expressed as "equivalent oxide thickness": although the
25 alternative material layer may be thick, it has the equivalent

effect of a much thinner layer of silicon dioxide (commonly called simply "oxide"). Many, if not most, of the attractive alternatives for achieving low equivalent oxide thicknesses are metal oxides, such as tantalum pentoxide and barium strontium titanate.

Researchers have found formation of such metal oxides as gate dielectrics to be problematic. At typical metal oxide deposition temperatures, the oxygen ambient or oxygen-containing precursor required to form them tends to also oxidize the silicon substrate, producing an oxide layer at the interface between the substrate and the gate dielectric. The presence of this interfacial oxide layer increases the effective oxide thickness, reducing the effectiveness of the alternative gate dielectric approach. The existence of the interfacial oxide layer places an ultimate constraint on the performance of an alternative dielectric field effect device.

SUMMARY OF THE INVENTION

The present invention comprises a semiconductor device structure utilizing a metal silicate gate dielectric layer, and a method for making the same. With the present invention, a metal silicate gate dielectric may be formed with a dielectric constant substantially higher than that of either conventional thermal silicon dioxide or silicon nitride dielectrics, and thus the metal silicate dielectric layer may be made substantially

thicker than a conventional gate dielectric with equivalent field effect. However, it is believed that the present invention largely avoids disadvantages, such as interfacial silicon dioxide formation and high interface state densities, that are found with conventional alternative dielectrics.

The present invention generally avoids the problems of other alternative dielectrics by employing an oxidized dielectric material comprising a significant amount of silicon, particularly at the silicon/dielectric interface. In one preferred embodiment, a graded silicate layer is formed, such that near the silicon interface the silicate layer has a large SiO_2 component, while the upper portion of the silicate layer has a large metal oxide component. Such a structure employs primarily SiO_2 bonding at the silicon interface, with resulting low interface state densities. However, the high atomic number metal included in the silicate layer can significantly increase the dielectric constant of the film. The present invention also provides for amorphous silicate gate dielectrics, which have dense microstructures and avoid many of the problems associated with grain boundaries in polycrystalline dielectrics.

In one aspect of the invention, a method of fabricating a semiconductor device is disclosed that comprises providing a single-crystal silicon substrate, forming a metal silicate dielectric layer on the substrate, and forming a conductive gate overlying the metal silicate dielectric layer. This method may

comprise one of several methods for forming the metal silicate dielectric layer. For example, a metal may be deposited on a cleaned Si surface, annealed to form a silicide layer, and then oxidized. Or, metal may be deposited on the substrate in an oxidizing ambient, followed by annealing in an oxidizing ambient. Or, metal and silicon may both be deposited on the substrate in a manner otherwise similar to one of the preceding procedures.

In another aspect of the invention, an integrated circuit having a field effect device fabricated thereon is disclosed that comprises a single-crystal silicon semiconducting channel region, a metal silicate gate dielectric overlying this channel region, and a conductive gate overlying this gate dielectric. The gate dielectric may be either an amorphous or a polycrystalline film. The metal silicate may be, for example, zirconium silicate, cerium silicate, zinc silicate, thorium silicate, bismuth silicate, hafnium silicate, lanthanum silicate, tantalum silicate, or a combination of these materials. Preferably, the metal silicate layer has a graded composition comprising a relatively greater ratio of silicon to metal near the semiconducting channel region, as compared to the ratio of silicon to metal near the conductive gate.

BRIEF DESCRIPTION OF THE DRAWINGS

This invention, including the features and advantages thereof, can be best understood by reference to the following drawings, wherein:

5 Fig. 1 is a cross-sectional view of a typical prior art integrated circuit field effect transistor;

 Figs. 2-5 are cross-sectional views of several semiconductor devices, illustrating different surfaces appropriate for deposition of a silicate gate dielectric
10 according to the invention;

 Figs. 6-9 are cross-sectional views of a semiconductor device during fabrication according to one preferred embodiment of the invention;

15 Figs. 10-12 are cross-sectional views of a semiconductor device during fabrication according to a second preferred embodiment of the invention;

 Figs. 13-15 are cross-sectional views of a semiconductor device during fabrication according to a third preferred embodiment of the invention; and

20 Figs. 16-18 are cross-sectional views of a semiconductor device during fabrication according to a fourth preferred embodiment of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

5 The preferred embodiments of the invention may be fabricated using a representative Si(100) substrate, as described herein. The description of these embodiments begins, as shown in Fig. 2, after formation of an epitaxial layer **22** on substrate **20** and implantation of an active channel region **24** in epitaxial layer **22**, and assumes that a protective or native silicon oxide region **26** (preferably comprising less than 1 nm of oxide) overlies channel **24** in the region of interest. Such a silicon oxide layer may be formed by heating a clean substrate to 600-700°C for approximately 30 seconds, in an oxygen ambient of $\sim 10^{-3}$ Torr. Processes for reaching this step in fabrication are all well-known in the art, as are various equivalents to which the present invention is applicable. The examples below assume that the channel **24** is formed in epi-layer **22**. However, the invention is equally applicable to gate dielectrics formed directly on substrate **20**, or other relatively pure Si structures. In the descriptions below, layers **20** and **22**, and region **24** will be used interchangeably, except where the context shows a particular item is meant.

The particular embodiment employed for forming a silicate gate dielectric will dictate whether silicon oxide region **26** will be either left in place and used in the formation of the silicate layer, removed such that the underlying silicon may be

used in the formation of the silicate layer, or removed and replaced with a passivation layer designed to inhibit interaction of the substrate in the metal silicate deposition process. The immediately following description relates to the preparation of the substrate for deposition of silicate-forming materials, and is applicable to the specific embodiments presented thereafter. There are two preferred starting surfaces for the invention if silicon oxide region **26** is to be removed. Region **26** may be removed so as to leave either a clean, bare upper surface **28** as shown in Fig. 3, or a hydrogen-terminated surface as shown in Fig. 4. If oxide region **26** is removed, the bare surface is preferred to the hydrogen-terminated surface if chemical reaction of the highly reactive Si surface can be prevented, e.g. by processing in ultrahigh (less than $\sim 10^{-8}$ Torr) vacuum until a point in the particular process where exposure to oxygen can be tolerated. Otherwise, the bare Si surface should be terminated with a suitable passivant, such as hydrogen, which inhibits reoxidation and yet may be readily removed at an appropriate point in the process.

The method of oxide removal is not believed to be critical to the practice of the invention, as long as a clean, oxide-free surface can be maintained until an overlying deposition is performed. One preferred method of performing removal of oxide **26** is by exposure to wet HF, for example by dipping the substrate in dilute HF for 30 seconds and rinsing in deionized

water. This both removes the native oxide and hydrogen terminates the surface. Another preferred method is by exposure to HF vapor; this provides similar results, but may be used, e.g., in a cluster tool to further prevent reoxidation or contamination of the surface. Either of these approaches may comprise other appropriate stripping chemicals, with HF or a NH_4F solution being preferred as a last step to provide termination.

Several other methods produce a non-terminated surface **28**, as shown in Fig. 3. One such method with particular applicability to cluster-tool practice is Si flux desorption; it has been found that below 10^{-8} Torr and at 780°C , an Si flux of preferably 1.5 \AA/sec for about 600 seconds not only removes native oxide, but produces an atomically smooth, stepped surface that may have advantages for ultrathin gate dielectrics. The alternative is simple desorption by heating of the substrate to high temperature in vacuum or in an H_2 ambient; it is believed, however, that the Si-flux method results in a superior surface structure. In any of these methods, if the substrate is not to be kept in ultrahigh vacuum until an overlying deposition is completed, surface **28** may be hydrogen terminated, e.g. by exposure to atomic hydrogen produced by a plasma or hot filament in an H_2 ambient.

Surface **28** may also be passivated with an ultrathin layer, such as a silicon nitride or silicon oxynitride layer, that is

not, strictly speaking, an oxide of silicon. Such layers act as a diffusion barrier and provide oxidation resistance to the substrate during formation of the overlying silicate layer. If an oxynitride layer is used, the preferred method of

5 oxynitridation is by exposure to NO. Oxynitrides produced by other methods are not believed to provide sufficient oxidation resistance at the required thicknesses to complete some of the gate dielectric structures disclosed herein, and/or require higher process temperatures, and as such are not preferred. For
10 instance, N₂O processes result in a much smaller incorporation of N than NO processes. NH₃ processes require a pre-existing SiO₂ film, and thus a uniform sub-nanometer oxynitride film appears to be difficult to achieve using NH₃. Additionally, NH₃ annealing apparently incorporates undesirable hydrogen into the
15 film structure.

A typical NO process applicable to the present invention is as follows. The substrate is cleaned to remove the pad oxide. As a final step in the cleaning, the substrate is dipped in dilute HF for 30 seconds, and rinsed in deionized water. The
20 substrate is then placed in a reaction chamber, which is then evacuated to 3×10^{-8} Torr, and then the substrate is heated to 500°C to remove the hydrogen passivation from the substrate surface. The substrate is heated to 700°C, and NO at 4 Torr is introduced into the chamber for 10 seconds to form the
25 oxynitride passivation layer. Fig. 5 depicts a passivation

layer 30, e.g., either an oxynitride or a nitride passivation layer.

Once the substrate has been prepared to provide either a clean Si surface, an oxide layer, or a protective barrier layer as described above, a metal silicate gate dielectric is formed on the substrate by one of several methods. Although the specific embodiments for gate dielectric formation described below may be readily adapted to the deposition of a wide range of metal silicate compositions and structures, the preferred metal silicate compositions and structures contain several properties as described below.

First, the metal silicate is preferably stable next to silicon. Appropriate silicates generally have a heat of formation that is more negative than the heat of formation of silicon dioxide, as this is believed to form a more stable gate structure and avoid the preferential formation of interfacial silicon dioxide. Some examples of these silicates are those of Ba, La, Hf, and the rare earth elements. Silicates with heat of formations close to that of SiO_2 (e.g. silicates of Sr, Y, Zr, Ta) may also be useful in the present invention, although stability of these silicates is generally less than that of silicates of the first group. Table 1 lists several candidates for this layer in order of heat of formation, with silicon dioxide included for comparison purposes.

Table 1

Material	Heat of Formation (kcal/g/atom of O)
Ca ₃ SiO ₅	-138
Ca ₂ SiO ₄	-135
Ba ₂ SiO ₄	-124
CaSiO ₃	-123
SrSiO ₃	-123
Mg ₂ SiO ₄	-122
Na ₂ SiO ₃	-121
BaSiO ₃	-120
MgSiO ₃	-119
ZrSiO ₄	-115
CeSiO ₄	-115
SiO ₂	-103

Second, it is preferred that the metal silicate have a high dielectric constant as compared to the dielectric constant of silicon dioxide (~4) or the dielectric constant of silicon nitride (~7). Generally, the dielectric constant of silicates increases with the atomic number of the metal included; higher atomic weight metals such as Ba, La, Hf, and the rare earth elements are therefore preferred.

Third, the silicate may be formed as either a polycrystalline or an amorphous film. Generally, polycrystalline films will have better dielectric constant. However, amorphous films generally have higher breakdown performance, form a better diffusion barrier, and have lower interface state densities. Also, with many of the preferred embodiments for formation of a silicate dielectric according to the present invention, formation of an amorphous film may be

easier than formation of a polycrystalline film because of the uniform stoichiometry required for a polycrystalline film.

Amorphous silicate films may also be stabilized by the inclusion of more than one metal in a mixed-metal silicate film.

5 ¹⁵ 7 Finally, the present invention comprehends a graded dielectric composition. In a preferred embodiment, a silicate film may be formed where the ratio of silicon to metal varies as a function of depth in the film. For example, a graded silicate film may be formed that is mainly SiO₂ at the substrate interface (e.g. 2-10 mol% metal oxide), thus providing an interface with a quality similar to that obtained with pure SiO₂. The ratio of silicon to metal is decreased with a grading profile that results preferably in a greater percentage of metal oxide near the top of the gate dielectric film.

Embodiment 1

15 In one embodiment according to the invention, a metal silicate gate dielectric is formed by depositing metal on a clean Si surface, annealing this structure to form a metal silicide, oxidizing the silicide layer, and annealing this structure. In this embodiment, a substrate such as shown in either Fig. 3 or Fig. 4 is used. If surface 28 is passivated as shown in Fig. 4, the substrate can be briefly heated to above 500°C in vacuum or an inert ambient to remove the passivation.

Referring to Fig. 6, a metal layer **32** (e.g. zirconium or hafnium) is deposited directly on surface **28**, e.g. by sputtering, evaporation, chemical vapor deposition (CVD) or plasma CVD. Sputter deposition is preferably done with a low-energy plasma system, such as collimated or long-throw sputtering; it should be noted that low deposition rates (e.g. on the order of a few angstroms per second) are preferred, as the total thickness to be deposited is small and uniformity is desired. For an 8" wafer, deposition may be completed in a system with a base pressure of $\sim 10^{-8}$ Torr, an operating pressure of $\sim 10^{-4}$ Torr, and a separation between the sputter gun and the wafer of 16 inches, and the wafer may be rotated to improve uniformity. Ar is an acceptable sputter gas, and the wafer may be maintained at a temperature of 400°C during deposition.

As an alternative to sputtering, metal layer **32** may be deposited by evaporation from an e-beam source onto a substrate at 500°C, with a net deposition rate on the order of tenths of angstroms to a few angstroms per second. The substrate is preferably rotated to improve uniformity. Other alternative methods include CVD or plasma CVD using appropriate precursors, such as zirconium tetrachloride and hydrogen gas. Again, with these methods low deposition rates and temperatures (600°C and lower) are preferred, and a downstream plasma type reactor is preferred to a reactor where the plasma is generated at the substrate.

Referring to Fig. 7, a metal silicide layer **34** is formed by annealing substrate **20** with metal layer **32** in an inert ambient, a reducing ambient, or vacuum. Although exact values will depend on the metal selected and the thickness of silicide desired, a 20 second anneal at 700°C in vacuum will generally suffice. During most silicide processes, silicon from substrate **20** diffuses into metal layer **32** to form metal silicide layer **34**. It should be noted that with this technique, an excessively thick metal layer **32** may be deposited, such that less than the entire layer **32** is converted to silicide during the anneal. In this case, the thickness of the silicide is controlled by the anneal time, and the excess metal is etched away after the silicide anneal step.

Referring now to Fig. 8, silicide layer **34** is converted to a silicate layer **36** by oxidation. Control of oxidation is critical during this step, as under-oxidation will result in decreased resistivity and over-oxidation may result in decreased capacitance for layer **36** (due to oxidation of the underlying silicon). Many oxygen anneal processes are available for this step, such as a low temperature O₂ anneal with or without ultraviolet exposure, or an activated oxygen anneal such as O₃, O₃ with ultraviolet exposure, a downstream O₂ plasma, N₂O, or a low temperature O₂ plasma with a DC-biased substrate. As an example of this last process, a downstream 1500W ECR source

operating at 1 mTorr, coupled with ~60V DC and 13.56 MHz or 300 kHz RF applied to the substrate may be used while He backside cooling at 80°C is also applied to the substrate. Processing time is determined experimentally such that both resistivity and dielectric constant lie within an acceptable range.

Generally, a high temperature anneal of silicate layer 36 is selected to densify or crystallize the film after low temperature oxidation. For example, the substrate may be densified by annealing in Ar for 20 seconds at 750°C. This

anneal may be done in either an inert or a reducing environment, with a reducing environment particularly useful where metal layer 32 was deposited by CVD using halogens. If a reducing environment is used, an additional low-temperature post-anneal in oxygen may be used to improve dielectric properties of silicate layer 36.

Finally, with reference to Fig. 9, conductive gate 38 is deposited over silicate gate dielectric 36. Processes for depositing gate 38 are well known in the art; gate 38 may be formed, by way of example, of doped polysilicon, metal, or a conductive metal oxide. As a variation on this embodiment, the silicide and oxidation steps may be combined, either by introducing an oxidizing ambient before the silicide is completely formed, or by completely overlapping the two steps. In this latter variation, a substrate such as that depicted in

Fig. 2 is preferable, as silicon oxide layer 26 can supply both oxygen and silicon towards the formation of silicate layer 36.

Embodiment 2

5 In a second embodiment according to the invention, a metal silicate gate dielectric is formed by depositing metal on a substrate in an oxidizing ambient, followed by annealing. This embodiment preferably utilizes a substrate prepared by one of the methods corresponding to Fig. 2, 3, or 4, and the metal may
10 be deposited by one of the methods described in Embodiment 1, with the following differences.

Referring to Fig. 10, an oxidized metal layer 40 may be deposited on a clean Si surface by sputtering as described above. However, some amount of controlled oxygen activity is
15 used to at least partially oxidize layer 40 as metal is supplied to the substrate. For example, O₂ or H₂O+H₂ may be introduced near the substrate during sputtering with Ar, with an O₂ flow rate of about one-tenth that of the Ar flow rate. For a metal deposition rate of 0.1 nanometers per second, the oxidizing gas
20 is preferably introduced from 0 to 5 seconds after the start of the deposition process.

If oxidized metal layer 40 is produced by the evaporation method, the oxidizer is preferably added near the substrate. To achieve near complete oxidation of the deposited metal, ~5-10
25 Torr of O₂ may be used for a metal deposition rate of 0.1

nm/sec. If a CVD method is used, appropriate precursors should provide the necessary oxygen (e.g. zirconium tetrachloride and water).

Referring to Fig. 11, layer 40 is reacted with the substrate to form metal silicate layer 36. Preferably, this is accomplished with a low-temperature oxygen anneal followed by a high temperature anneal, such as those described in the preceding embodiment. One example of a preferred oxygen anneal is a 400°C anneal in O₃ for 60 seconds. ✓

It should be noted that this embodiment may be readily tailored to produce a graded silicate layer. One variation on this method is shown in Fig. 12, wherein layer 40 is deposited over a silicon oxide layer 26. In such an embodiment, oxygen activity during the anneal may be reduced, and silicate layer 36 may be formed by "stealing" both oxygen and silicon from layer 26. The grading of the structure may be adjusted by adjusting the relative initial thicknesses of layers 26 and 40. It may also be appropriate to supply Si to layer 40 by implantation of energetic ions from a remote plasma, using DC bias on the substrate to adjust penetration depth. For example, silane may be used to implant Si into layer 40.

Embodiment 3

In a third embodiment according to the invention, a metal silicate gate dielectric is formed by depositing both metal and silicon on the substrate in an oxidizing ambient, followed by annealing. In this embodiment, the substrate preparation may be chosen as any of those shown in Figs. 2-5. As this method generally does not rely on silicon from the substrate as a component of the silicate film, a surface that limits oxidation of the substrate, such as the diffusion barrier surface of Fig. 5, is preferred. The metal and silicon may be deposited by one of the methods described in Embodiment 1, with the following differences.

Referring to Fig. 13, an oxidized metal and silicon layer **42** may be deposited on a clean Si surface by sputtering as described in Embodiment 2 for the deposition of oxidized metal layer **40**. The deposition of both metal and silicon is accomplished by replacing the metal target with an appropriate silicide target. The disadvantage of this method is that deposition of a graded layer from a single composition target is difficult.

If oxidized metal and silicon layer **42** is produced by the evaporation method, a method similar to that of Embodiment 2 may be selected. In this case, it is preferred that separate metal and silicon e-beam sources be used such that the ratio of silicon to metal may be varied during deposition.

If a CVD method is used, appropriate precursors should provide the necessary oxygen. Some combinations of precursors, such as a combination of silane, zirconium tetrachloride, and oxygen, may be used to produce uniform stoichiometry layers but may be difficult to use for a graded composition layers. For a graded layer, CVD precursors such as a combination of silicon tetrachloride, zirconium tetrachloride, and water are preferred.

Formation of a high performance silicate layer using this process will generally require both a low-temperature oxygen anneal and a high temperature anneal such as those described in the preceding embodiments. Figs. 14 and 15 depict, respectively, layer **42** deposited on a silicon oxide layer **26** and on a diffusion barrier layer **30** (e.g. a silicon oxynitride layer). As noted, the presence of the diffusion barrier layer **30** allows for the selection of a more aggressive oxygen anneal.

Embodiment 4

In a fourth embodiment according to the invention, a metal silicate dielectric is formed by depositing both metal and silicon on the substrate, followed by annealing. Silicates formed according to this embodiment may be formed on a substrate prepared according to Figs. 2, 3, 4, or 5. In its most straightforward form, this embodiment is a combination of the metal deposition/silicide technique of Embodiment 1 with the

metal/silicon deposition sources of Embodiment 3, such that a silicide is deposited directly.

Referring to Fig. 16, a metal silicide layer **44** may be deposited on a clean Si surface by sputtering as described in Embodiment 1 for the deposition of metal layer **34**. The deposition of both metal and silicon is accomplished by replacing the metal target with an appropriate silicide target. The disadvantage of this method is that deposition of a graded layer from a single composition target is difficult.

If metal silicide layer **44** is produced by the evaporation method, a method similar to that of Embodiment 1 may be selected. In this case, it is preferred that separate metal and silicon e-beam sources be used such that the ratio of silicon to metal may be varied during deposition.

If a CVD method is used, appropriate precursors should provide the necessary oxygen. Some combinations of precursors, such as a combination of silane and zirconium tetrachloride, may be used to produce uniform stoichiometry layers but may be difficult to use for a graded composition layers. For a graded layer, CVD precursors such as a combination of silicon tetrachloride, zirconium tetrachloride, and hydrogen are preferred. Excess hydrogen may be required to prevent the incorporation of chlorine into the film.

Formation of a high performance silicate layer **46** (Fig. 17) from layer **44** using this process will generally require both a

low-temperature oxygen anneal and a high temperature anneal such as those described in the preceding embodiments, particularly Embodiment 1. As noted in the previous embodiment, the presence of a diffusion barrier layer **30** allows for the selection of a more aggressive oxygen anneal.

Embodiment 5

In a fifth embodiment according to the invention, a metal silicate dielectric is formed by depositing both a metal oxide and silicon on the substrate, followed by oxygen annealing. This approach sometimes works better than the silicide approaches above, since the deposited layer is not in a highly reduced (i.e. oxygen deficient) state, at least to the same degree as with the silicide intermediary approaches.

Silicates formed according to this embodiment may be formed on a substrate prepared according to Figs. 2, 3, 4, or 5.

Referring to Fig. 19, a partially reduced metal silicate layer **50** may be deposited on a clean Si surface by co-sputtering a metal oxide, such as ZrO_2 and elemental Si, to form oxygen-deficient zirconium silicate. Alternatively, artisans may co-sputter HfO_2 and Si, to form oxygen-deficient hafnium silicate. Although this zirconium silicate is partially reduced, it may be more readily oxidized to a full silicate than zirconium silicide may be fully oxidized.

For an 8" wafer, deposition may be completed in a system with a base pressure of $\sim 10^{-8}$ Torr, an operating pressure of $\sim 10^{-3}$ Torr, and a separation between the sputter gun and the wafer of 16 inches, and the wafer may be rotated to improve uniformity. Ar or a mixture of Ar and O_2 ($O_2 \sim 10-50\%$) is an acceptable sputter gas, and the wafer may be maintained at a temperature of 400-500°C during deposition. The RF power setting should be low, at about 50-100 watts, to avoid particle and defect formation. The Si power settings are not usually as important, thus they can be set the same as the ZrO_2 settings.

As an alternative to sputtering, a partially reduced metal silicate layer **50** may be deposited by evaporation from separate zirconium oxide and silicon e-beam sources onto a substrate at 500-600°C, with a net deposition rate on the order of tenths of angstroms to a few angstroms per second. The substrate is preferably rotated to improve uniformity.

Referring now to Fig. 8, partially reduced metal silicate layer **50** is converted to a silicate layer **52** by oxidation. Control of oxidation is critical during this step, as under-oxidation will result in decreased resistivity and over-oxidation may result in decreased capacitance for layer **52** (due to oxidation of the underlying silicon). Post-anneals in O_2 at about 400-550° for up to about 30 minutes generally increase capacitance while maintaining low leakage current. Anneals at higher temperatures or longer times tend to degrade capacitance.

Many oxygen anneal processes are available for this step, such as a low temperature O₂ anneal, with or without ultraviolet exposure, or an activated oxygen anneal such as O₃, O₃ with ultraviolet exposure, a downstream O₂ plasma, N₂O, or a low

5 temperature O₂ plasma with a DC-biased substrate. As an approximate example of this last process, a downstream 1500W ECR source operating at 1 mTorr, coupled with ~60V DC and 13.56 MHz or 300 kHz RF applied to the substrate may be used while He backside cooling at 80°C is also applied to the substrate.

10 Processing time is determined experimentally such that both resistivity and dielectric constant lie within an acceptable range.

Generally, a high temperature anneal of silicate layer **52** is selected to densify or crystallize the film after low

15 temperature oxidation. For example, the substrate may be densified by annealing in Ar for **20** seconds at **750°C**. This anneal may be done in either an inert, reducing or an oxidizing environment, with a reducing environment particularly useful where partially reduced metal silicate layer **50** was deposited by

20 CVD using halogens. If a reducing environment is used, an additional low-temperature post-anneal in oxygen may be used to improve dielectric properties of silicate layer **52**. For physical vapor deposited (PVD) dielectrics, an inert or oxidizing ambient is generally preferred. As noted in a

previous embodiment, the presence of a diffusion barrier layer
30 allows for the selection of a more aggressive oxygen anneal.
The independent introduction of the metal oxide, such as ZrO_2 ,
and the silicon allows for direct control of a graded metal-to-
5 silicon profile of the silicate dielectric.

We have found that, for gate dielectrics, it is not
necessarily desirable to form exactly stoichiometric $ZrSiO_4$.
Instead, it is sometimes preferable to form slightly Zr-rich or
Zr-deficient films. Stoichiometric $ZrSiO_4$ will crystallize more
10 easily, but non-stoichiometric films remain more stable in
amorphous phases. Further, controlling the Zr-content allows
control of the dielectric constant, as well as SiO_2 -like
interface properties. Oxygen-rich silicates seem to exhibit
lower leakage currents and better interface properties, because
15 a more SiO_2 -like interface and film improves both.

In a variation of this embodiment, it is possible to make
slight changes to the oxygen content of the partially reduced
metal silicate layer 50. A slightly higher oxygen content can
be obtained by substituting SiO_2 for the Si in either the
20 sputtering or evaporation processes. This SiO_2 sputtering will
form SiO, which will thus provide additional oxygen beyond the
 ZrO_2 and Si, yet not provide enough oxygen to form
stoichiometric $ZrSiO_4$.

It is often desirable to form an only slightly reduced
25 metal silicate layer. However, sometimes, it may be preferable

to initially form a more reduced, but not fully reduced metal silicate layer 50. In these instances, the ZrO_2 can be replaced with Zr, while the Si is replaced by SiO_2 . The resulting SiO provides the silicate with more oxygen than the silicide methods described above, but less than the ZrO_2/Si method of embodiment 5.

Embodiment 6

As an alternative to the preceding embodiments, it is recognized that some of the deposition steps described may be repeated to tailor the composition of a silicate layer. With reference to Figs. 17 and 18, for example, layer 46 may form only an intermediate layer. For example, one or more monolayers of either silicon, metal, or a combination may be deposited using the e-beam evaporation method described in Embodiment 4, followed by a short anneal in an oxidizing ambient to produce intermediate layer 46. This may then be followed by deposition of a second intermediate layer 48 by a similar process, with the same or a different composition. Using this method, oxidized silicon and oxidized metal layers can be interleaved in an alternating fashion prior to a final anneal. Or, graded compositions can be deposited directly.

The present invention is not limited by the specific embodiments described herein. Although a particular substrate and type of device have been described herein for clarity, this invention has application to Si devices generally which modify

the semiconducting characteristics of an active region using the field effect of an overlying conductive region. Various other combinations of the described steps may be used to produce silicate gate dielectrics, and such are intended to fall within
5 the scope of this invention.

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